

ABSTRACT OF THE DISCLOSURE

A layout of a memory cell of a dual-port semiconductor memory device provides for one memory cell that includes a total of eight transistors, including two NMOS scan transistors. Among the transistors, two PMOS transistors and six NMOS transistors are disposed in one N-well area and one contiguous P-well area of a semiconductor substrate, respectively. The N-well area is disposed at a corner of the memory cell for improving efficiency of the layout. Since one N-well area and one P-well area are formed in the semiconductor substrate, the size of an isolated area between the N-well area and the P-well area can be reduced, thus also reducing the size of a memory cell.